

Using the Evaluation Board

The ISL6410 and ISL6410A are synchronous current mode PWM regulators offering control and protection features.

The ISL6410, ISL6410A evaluation boards highlight the operation of the IC in embedded DC-DC converter applications. Table 1 shows the available evaluation boards.

TABLE 1. EVALUATION BOARDS

BOARD NAME	IC	PACKAGE
ISL6410EVAL1C	ISL6410IU	10 Ld MSOP
ISL6410AEVAL1A	ISL6410AIU	10 Ld MSOP

Recommended Test Equipment

- A 0V-10V, 5A capable power supply
- An electronic load
- Four channel oscilloscope with probes
- Precision digital multimeters

Power and Load Connections

Input Voltage - The ISL6410 operates at 3.3V \pm 10% and the ISL6410A operates at 5.0V \pm 10%. When connecting to a 0V-10V power supply, connect the positive lead of the power supply to VIN (P1) post and the ground lead of the supply to the GND (P2) post.

Output Adjustment

The Output Voltage can be adjusted to the levels shown in the table below by applying the appropriate logic level to the VSET pin via the jumper J2.

High = JP2 1-2 closed and JP2 2-3 open and

Low = JP2 2-3 open and JP2 2-3 closed.

VSET	ISL6410 Vo	ISL6410A Vo
High	1.8V	3.3V
Open (NC)	1.5V	1.8V
Low	1.2V	1.2V

Shutdown

The PWM can be shut down by pulling the EN pin low or the P6 terminal marked as EN.

SYNC Function

The ISL6410, ISL6410A can be synchronized to an external CMOS clock signal in the range of 500kHz to 1.0MHz. This is to be applied to the SYNC pin or Terminal marked as P7.

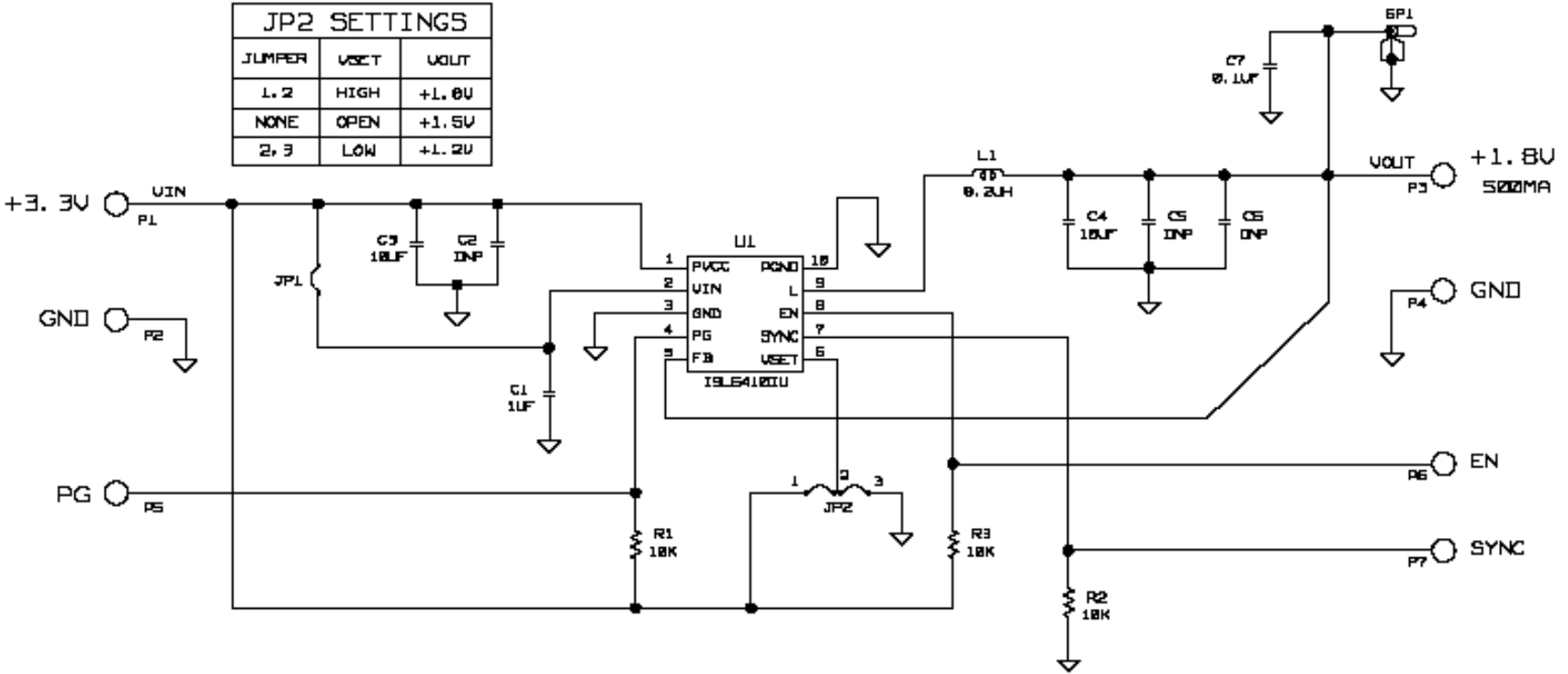
Power Good

When the PWM is within \pm 10% of the set value the PG signal will go high. The open drain PG pin is pulled HIGH to VIN by a resistor on the board. The PGOOD circuitry monitors VOUT via the FB pin to determine if the outputs are in regulation. PG can be monitored at terminal P8.

Overcurrent Protection

The switch current is internally limited to 1300mA max. No external adjustment is available.

ISL6410EVAL1C Schematic

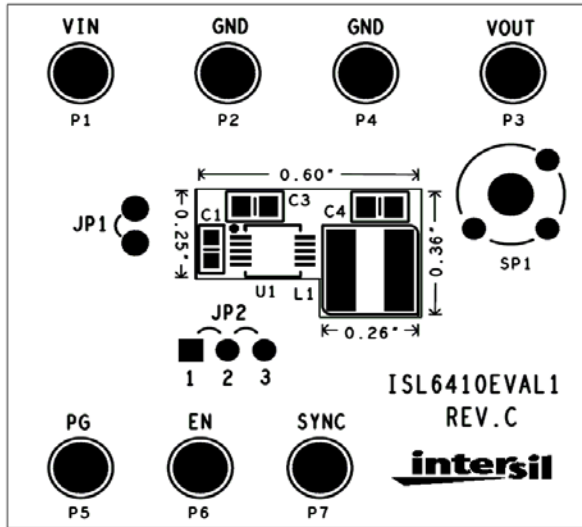


Application Note 1131

ISL6410EVAL1C Bill of Materials

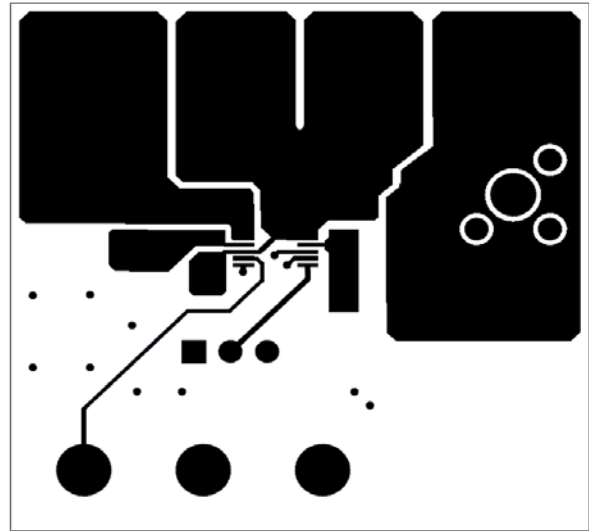
ITEM	REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	PKG.	VENDOR
1	U1	1	ISL6410IU	IC, Linear	Regulator, Single Synchronous Buck	10 Ld MSOP	Intersil
2	L1	1	MSS6122-822MX	Inductor	8.2μH, 20%, 1.25A	SMT	Coilcraft
3	C1	1	06036D105KAT2A	Capacitor, Ceramic, X5R	1μF, 10%, 6.3V	SM_0603	AVX/Generic
4	C2, C6	2	DNP	Capacitor, Ceramic		SM_0603	AVX/Generic
5	C3, C4	2	08056D106KAT2A	Capacitor, Ceramic, X5R	10μF, 10%, 6.3V	SM_0805	AVX/Generic
6	C5	1	DNP	Capacitor, Ceramic		SM_0805	AVX/Generic
7	C7	1	06036C104KAT2A	Capacitor, Ceramic, X7R	0.1μF, 10%, 6.3V	SM_0603	AVX/Generic
	Alternate		0603YC104KAT2A	Capacitor, Ceramic, X7R	0.1μF, 10%, 16V	SM_0603	AVX/Generic
8	R1, R2, R3	3		Resistor, Film	10kΩ, 5%, 1/16W	SM_0603	Panasonic/Generic
9	JP1	1	68000-236-1X2	Header	1X2 Break Strip GOLD		
10	JP2	1	68000-236-1X3	Header	1X3 Break Strip GOLD		
11	JP1, JP2	2	S9001-ND	Jumper	2 pin jumper		Digikey
12	SP1	1	TEK131-4353-00	Terminal, Scope Probe	Terminal, Scope Probe		Tektronix
13	P1 - P7	7	1514-2	Turrett Post	Terminal post,through hole, 1/4 inch tall	PTH	Keystone

ISL6410EVAL1C Layout



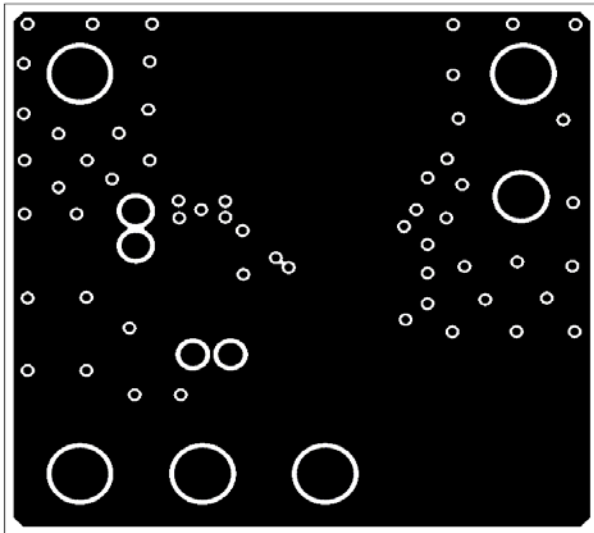
TOP SILK

SILKSCREEN TOP



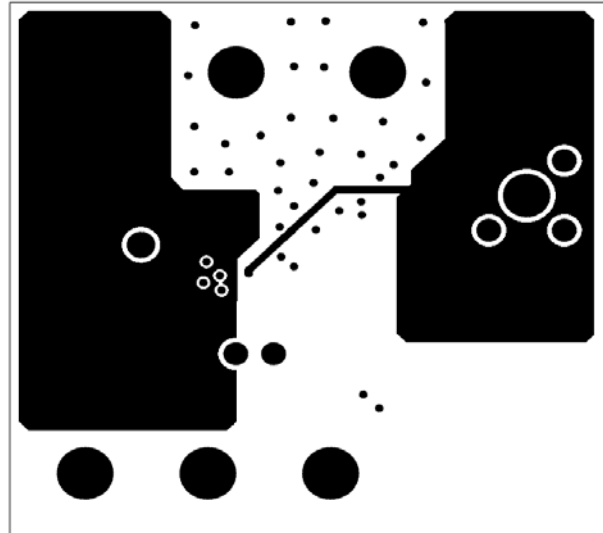
LAYER 1 (TOP SIDE)

LAYER 1



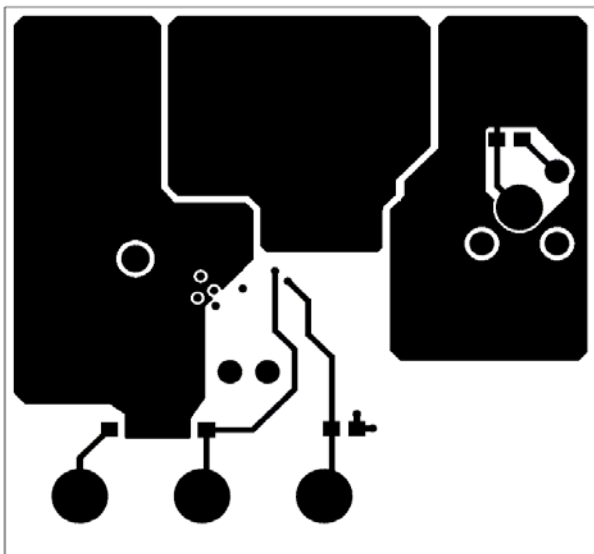
LAYER 2

LAYER 2



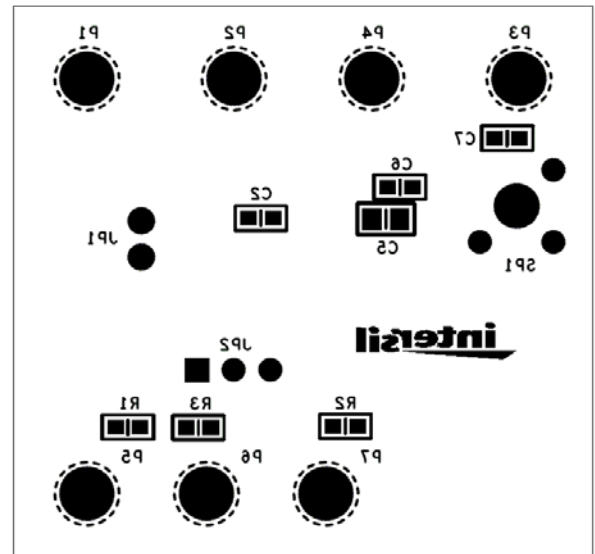
LAYER 3

LAYER 3



LAYER 4

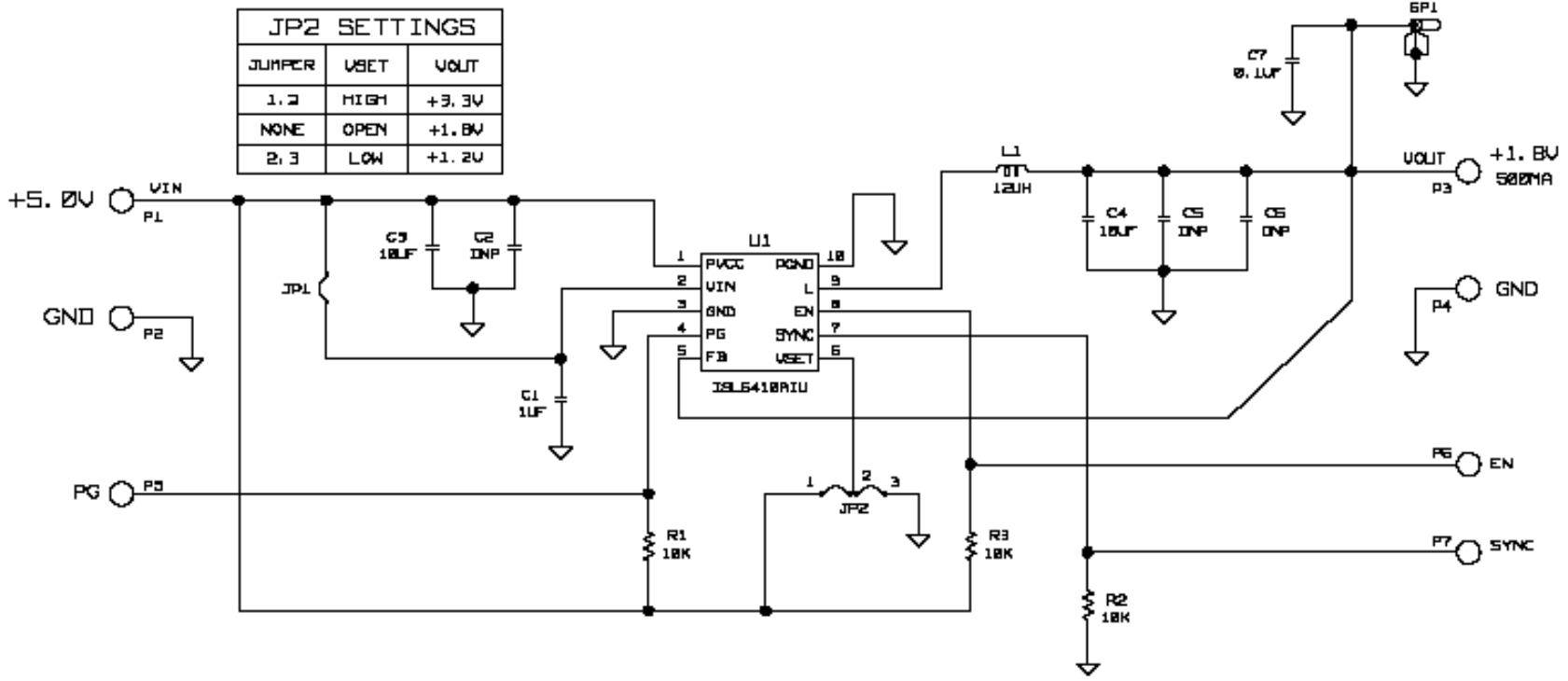
LAYER 4



BOTTOM SILK

SILKSCREEN BOTTOM

ISL6410AEVAL1A Schematic



Application Note 1131

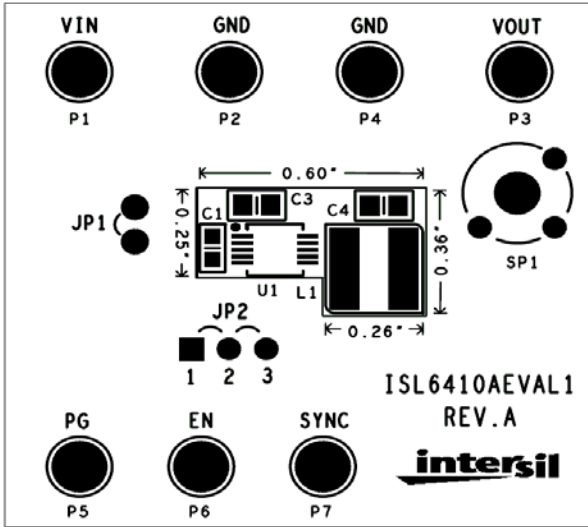
ISL6410AEVAL1A Bill of Materials

ITEM	REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	PKG.	VENDOR
1	U1	1	ISL6410IU	IC, Linear	Regulator, Single Synchronous Buck	10 Ld MSOP	Intersil
2	L1	1	MSS6122-822MX	Inductor	8.2μH, 20%, 1.25A	SMT	Coilcraft
3	C1	1	06036D105KAT2A	Capacitor, Ceramic, X5R	1μF, 10%, 6.3V	SM_0603	AVX/Generic
4	C2, C6	2	DNP	Capacitor, Ceramic		SM_0603	AVX/Generic
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6	C5	1	DNP	Capacitor, Ceramic		SM_0805	AVX/Generic
7	C7	1	06036C104KAT2A	Capacitor, Ceramic, X7R	0.1μF, 10%, 6.3V	SM_0603	AVX/Generic
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13	P1 - P7	7	1514-2	Turret Post	Terminal post, through hole, 1/4 inch tall	PTH	Keystone

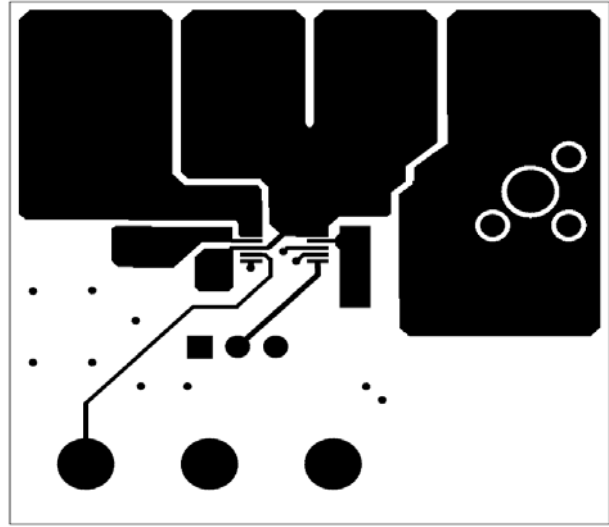
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ISL6410AEVAL1A Layout

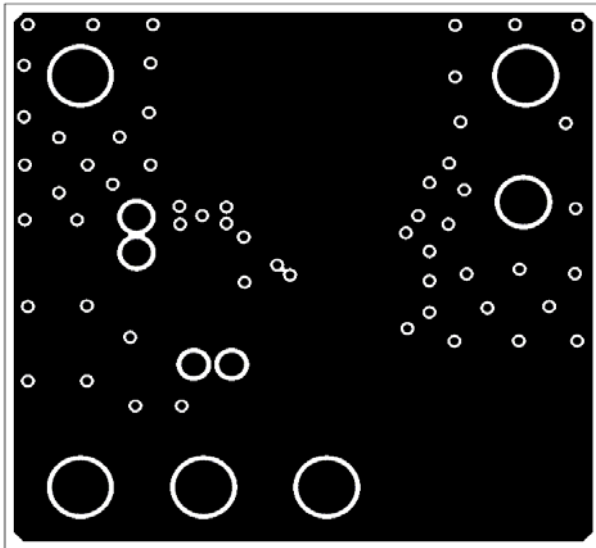


TOP SILK

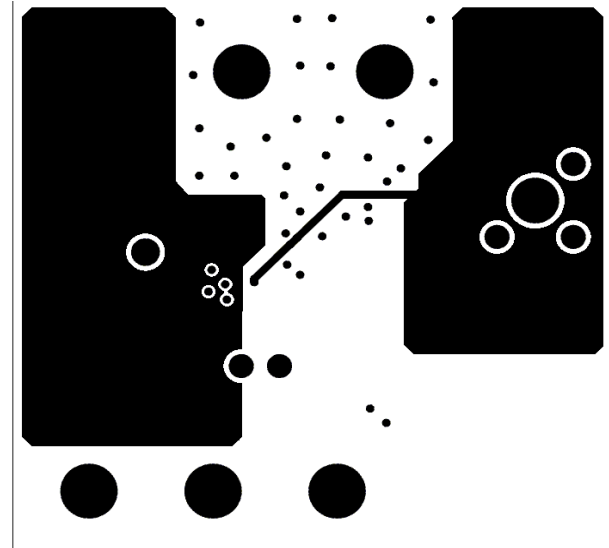


LAYER 1 (TOP SIDE)

SILKSCREEN TOP

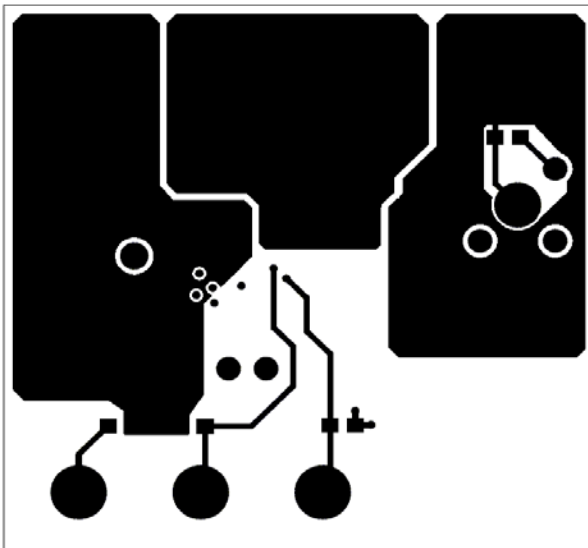


LAYER 2



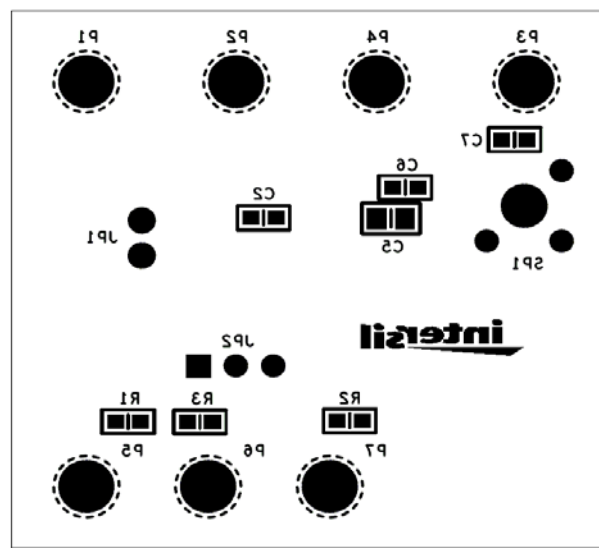
LAYER 3

LAYER 3



LAYER 4

LAYER 4



BOTTOM SILK

SILKSCREEN BOTTOM